AMBA AXI4

Aktuelle Trends bei System-on-Chip Bussen

Einführung

- Über mich
  - Hauptentwickler GECKO3main FPGA Applikationsmodul
  - Xilinx und MicroBlaze Anwender
- Motivation für das Thema AXI4
  - Voraussichtlich grosse Verschiebung bei IP Core Lieferanten
  - Öffnet Chance für praktikable Second-Source

Status bisher: SoC Busse

- Viele verschiedene Busse
  - CoreConnect (PLB4v6, PLB, OPB): IBM, Xilinx
  - Avalon (Memory Mapped, Stream): Altera
  - Wishbone: Lattice, Opencores.org
  - AMBA (AHB, APB, AXI): ARM, Gaissler
  - ClustraBus: Enclustra

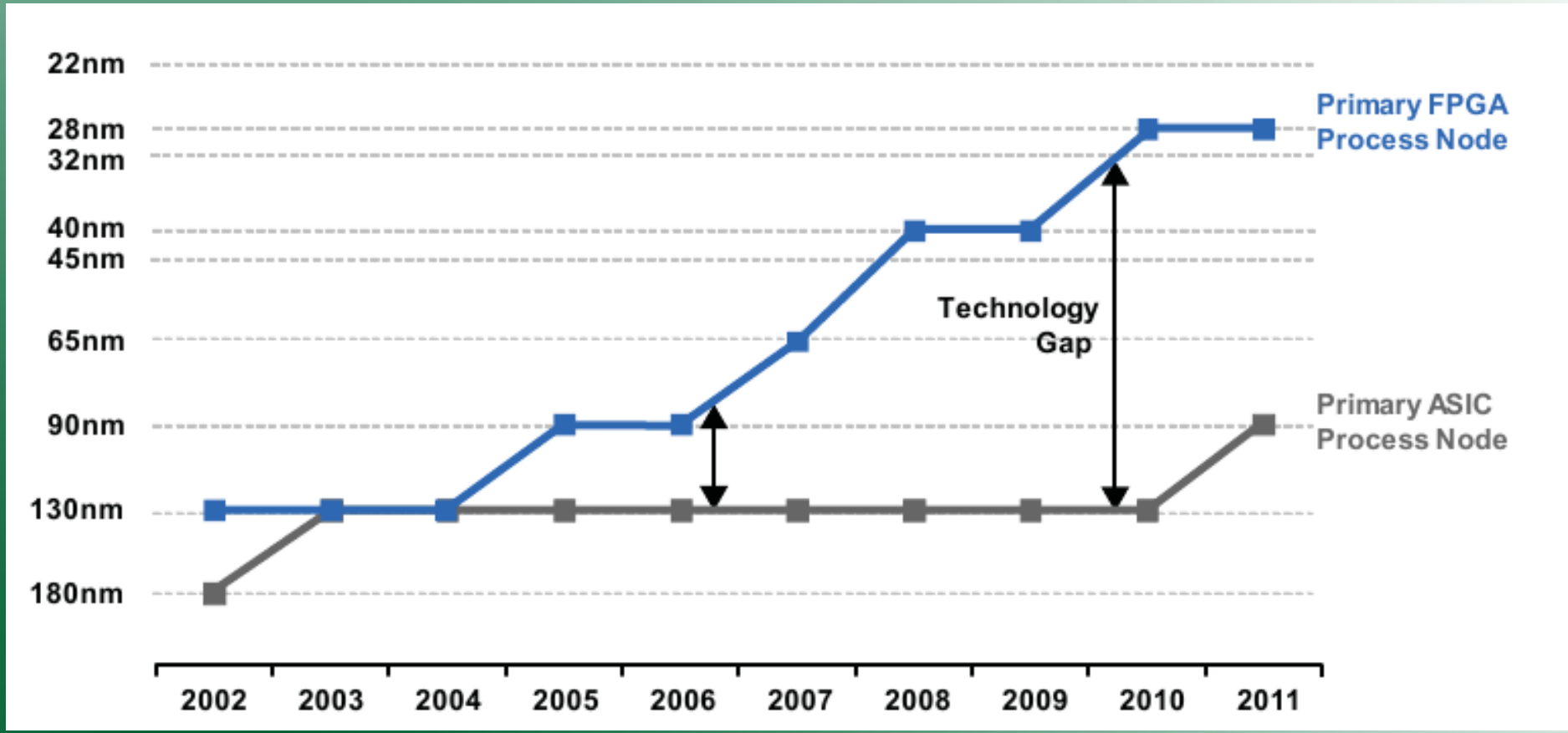
Status bisher: CPU im FPGA

- Hard Macro CPU
  - Für Hochgeschwindigkeitssysteme derzeit nur von Xilinx (PowerPC 440 in Virtex2pro, Virtex4FX oder Virtex5FXT)
- Soft Core CPU
  - Viele Varianten und Anbieter
  - Trotzdem Risiko von Lock-in Effekt:
    - Lizenzbedingungen
    - SoC Bus und dazugehörige IP Core Lieferanten

Der Wechsel

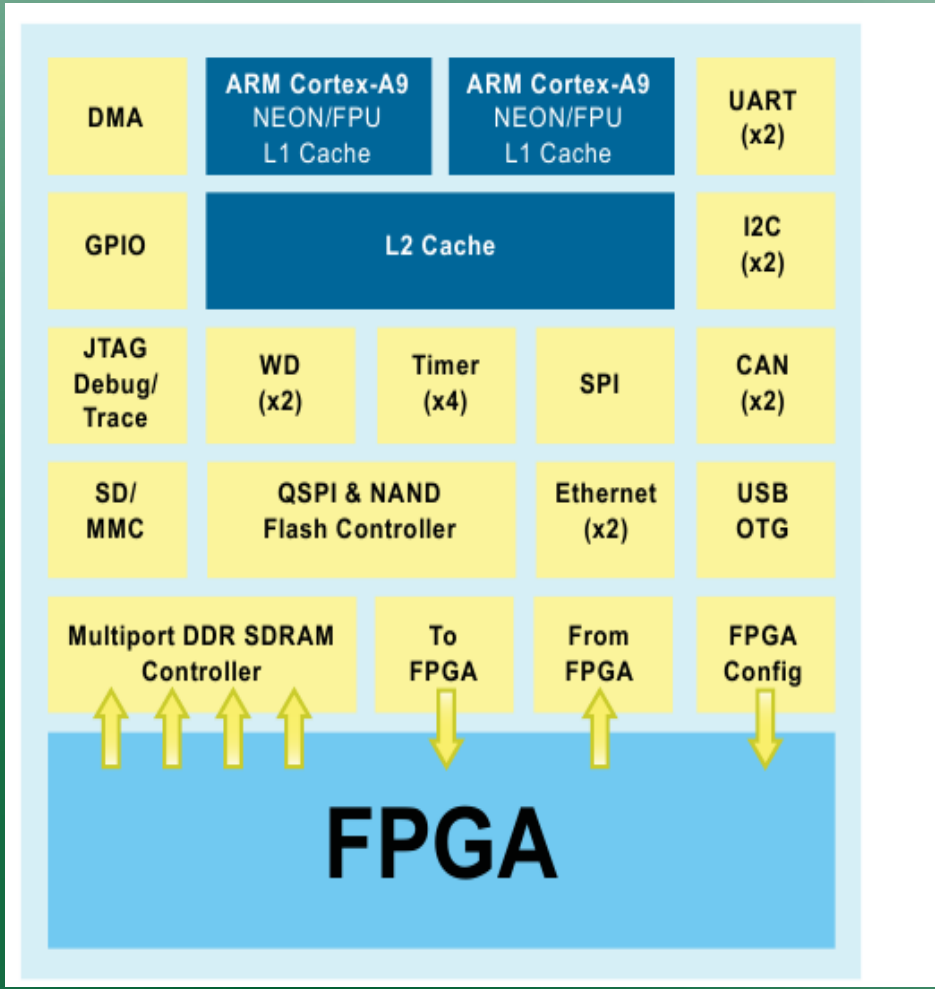
- Xilinx baut ab Virtex6 keine PowerPC Cores mehr ein
- Altera und Xilinx wechseln den SoC Bus: Neu verwenden beide AMBA AXI4
- Altera und Xilinx bauen FPGAs mit ARM Cortex-A9 Hard-Macro CPU in 28 nm

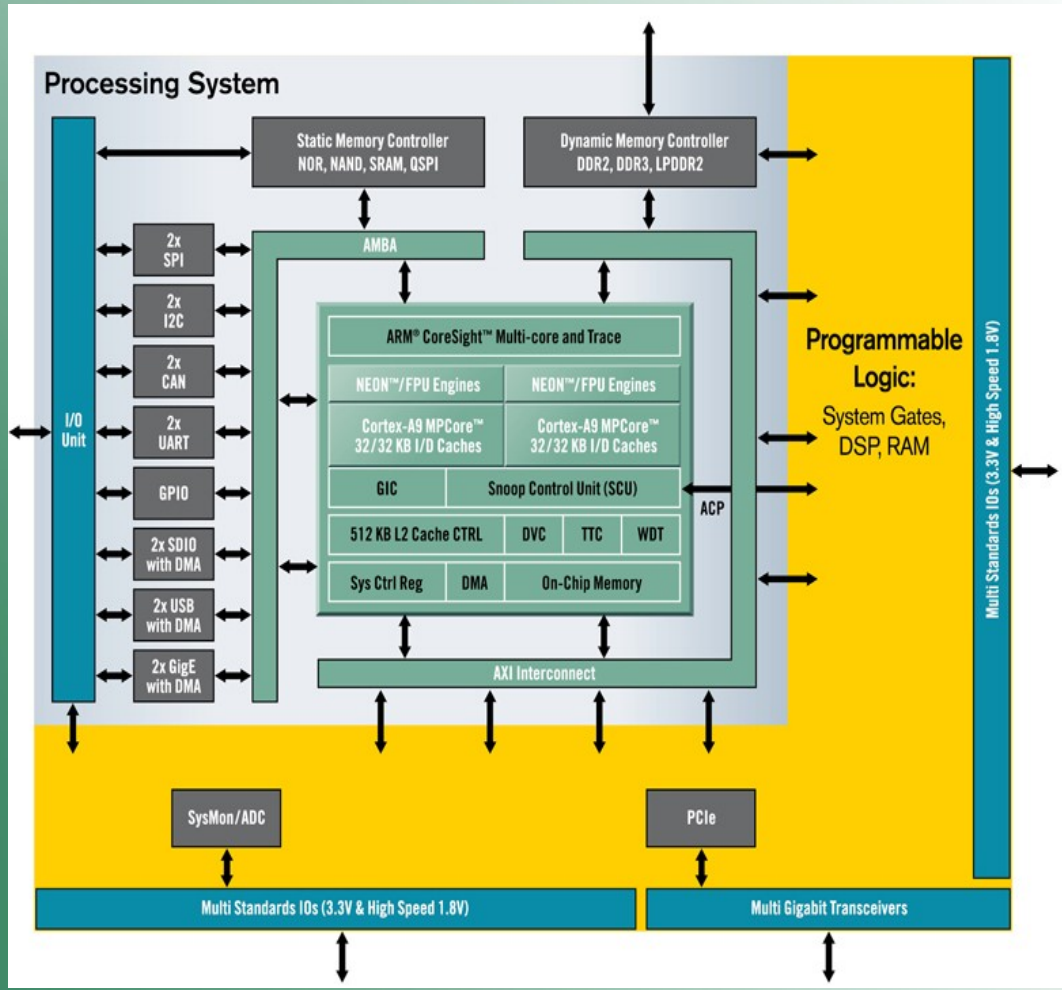
Strukturgrösse



- Quelle: Whitepaper Altera Strategic Considerations for Emerging SoC FPGAs

Altera vs. Xilinx





AXI4 Überblick

- AXI4—for high-performance memory-mapped requirements.
- AXI4-Lite—for simple, low-throughput memory-mapped communication (for example, to and from control and status registers).
- AXI4-Stream—for high-speed streaming data.

"Low power is also important to ARM, and the CoreLink Network Interconnect is no exception. The RTL has been optimized to make extensive use of automated clock gate insertion by synthesis tools. Implementation trials have shown that as many as 95% of the flops are clock gated when idle."

http://www.arm.com/products/system-ip/interconnect/axi/index.php

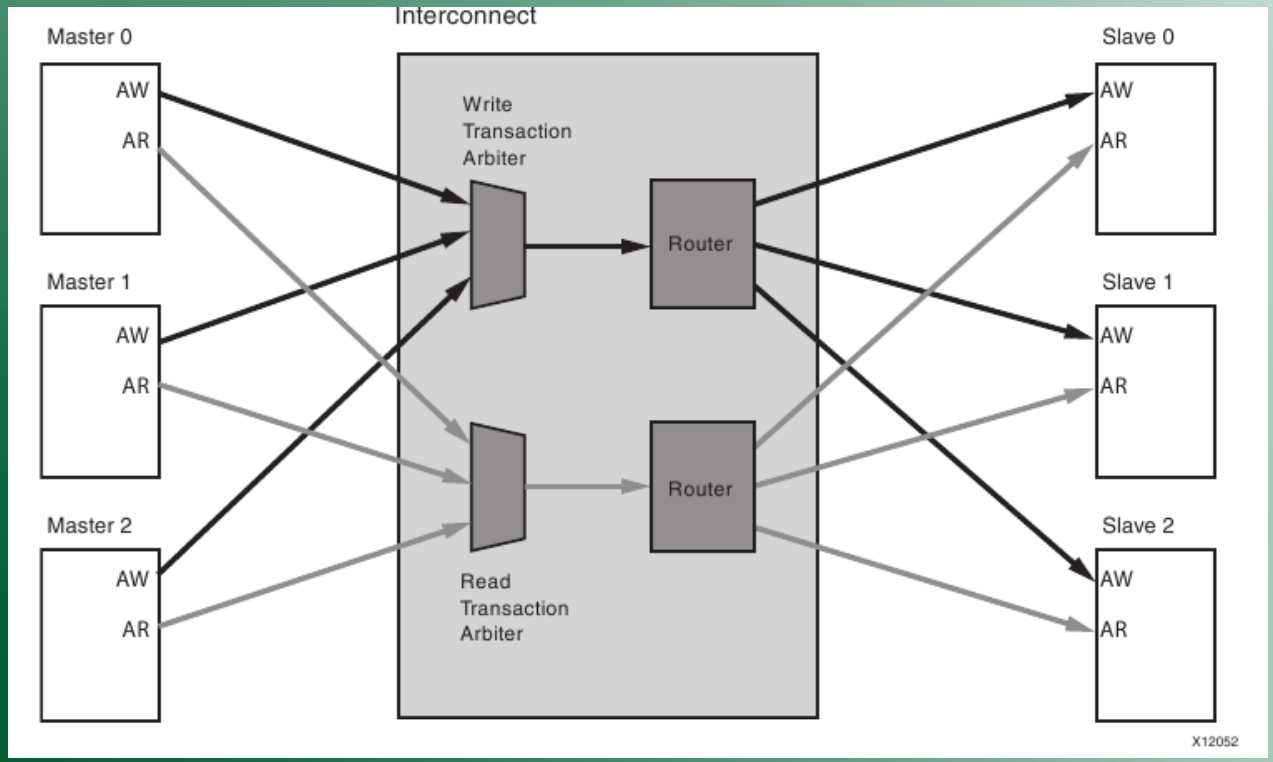
AXI4 Features

- Buswidth:
  - AXI4: Each master and slave connection can independently use data widths of 32, 64,128, or 256 bits wide

    AXI4-Lite: 32 bits 32-bit address width
- Burst lengths up to 256 (AXI4-MM)
- Built-in clock-rate and AXI4-Lite conversion
- Supports multiple outstanding transactions

AXI4 Zugriffssteuerung

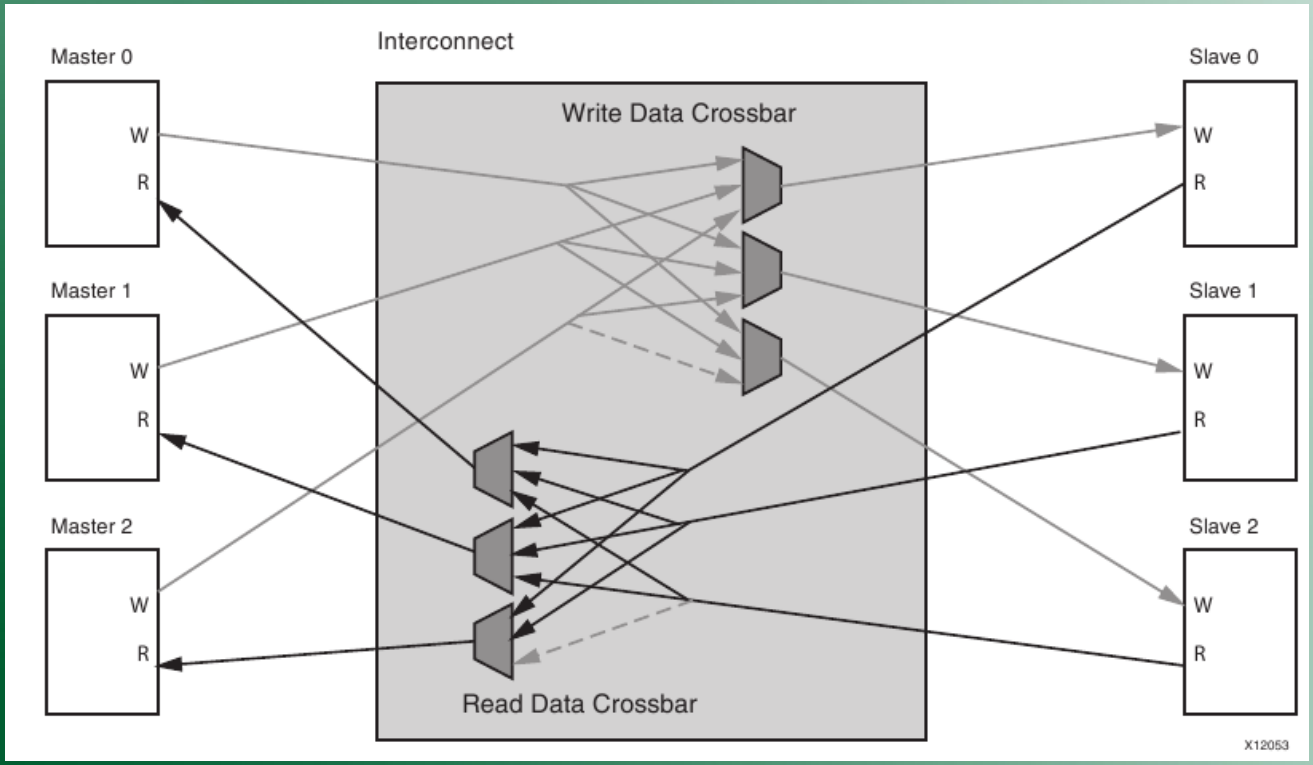
- Shared-Address, Multiple-Data (SAMD) crossbar
- Fixed priority and round-robin arbitration



- Quelle: Xilinx UG761 AXI Reference Guide User Guide

AXI4 Datenpfade

- Optional register-slice pipelining
- Optional data-path FIFO buffering



- Quelle: Xilinx UG761 AXI Reference Guide User Guide

Migration nach AXI4

Xilinx

- In EDK integriert (ab 12.3)
- MicroBlaze mit AXI
- Neu Little-Endian anstatt Big-Endian!
- Bridges zu PLBv4.6 vorhanden

Altera

- In Qsys integriert (Beta Version)
- Heterogenes System (Avalon parallel mit AXI)

Migration nach AXI4, Xilinx

Interface	Features	Replaces
AXI4	• Traditional memory mapped address/data interface. • Data burst support.	PLBv3.4/v4.6 OPB NPI XCL
AXI4-Lite	• Traditional memory mapped address/data interface. • Single data cycle only.	PLBv4.6 (singles only) DCR DRP
AXI4-Stream	• Data-only burst.	Local-Link DSP TRN (used in PCIe) FSL

- Quelle: Xilinx UG761 AXI Reference Guide User Guide

Soft Core CPU Support

CPU Typ	Hersteller	Bussystem	FPGA Support
MicroBlaze	Xilinx	AMBA AXI4, PLBv4.6	Nur Xilinx
Nios II	Altera	Avalon	Nur Altera
Leon (SPARC komp.)	Gaissler	AMBA AHB	Alle
Aemb (MicroBlaze komp.)	Aeste	Wishbone	Alle
LatticeMico32	Lattice	Wishbone	Alle
Cortex-M1	ARM	AMBA AHB-lite	Alle

Chancen für Leica

- Weiterhin freie Wahl des FPGA Herstellers
- Möglichkeit zum Aufbau einer konzernweiten IP Datenbank
- Möglichkeit zur Weiternutzung von Software Komponenten

Referenzen, Fragen

Xilinx Zynq-7000 EPP Product Brief
Xilinx UG761 AXI Reference Guide User Guide

Altera Strategic Considerations for Emerging SoC FPGAs
Altera Avalon Interface Specifications

http://en.wikipedia.org/wiki/CoreConnect

http://www.arm.com/products/system-ip/interconnect/axi/index.php
http://www.arm.com/products/processors/cortex-m/cortex-m1.php

Fragen?